

74LVXC3245

8-Bit Dual Supply Configurable Voltage Interface Transceiver with TRI-STATE® Outputs for 3V System

General Description

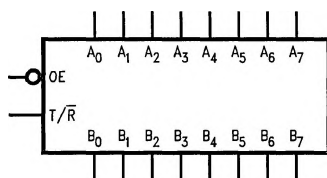
The LVXC3245 is a 24-pin dual-supply, 8-bit configurable voltage interface transceiver suited for PCMCIA and other real time configurable I/O applications. The V_{CCA} pin accepts a 3V supply level. The A port is a dedicated 3V port. The V_{CCB} pin accepts a 3V-to-5V supply level. The B port is configured to track the V_{CCB} supply level respectively. A 5V level on the V_{CC} pin will configure the I/O pins at a 5V level and a 3V V_{CC} will configure the I/O pins at a 3V level. The A port should interface with a 3V host system and the B port to the card slots. This device will allow the V_{CCB} voltage source pin and I/O pins on the B port to float when $\overline{OE}$ is HIGH. This feature is necessary to buffer data to and from a PCMCIA socket that permits PCMCIA cards to be inserted and removed during normal operation.

Features

- Bidirectional interface between 3V and 3V-to-5V buses
- Control inputs compatible with TTL level
- Outputs source/sink up to 24 mA
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Available in SOIC and QSOP packages
- Implements patented Quiet Series EMI reduction circuitry
- Flexible V_{CCB} operating range
- Allows B port and V_{CCB} to float simultaneously when $\overline{OE}$ is HIGH
- Functionally compatible with the 74 series 245

Ordering Code: See Section 11

Logic Symbol

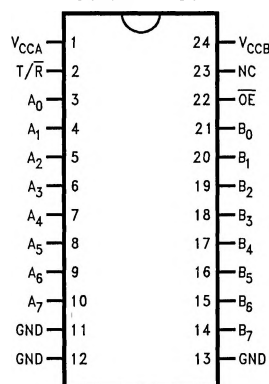


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Pin Names	Description
$\overline{OE}$	Output Enable Input
T/ $\overline{R}$	Transmit/Receive Input
A ₀ -A ₇	Side A Inputs or TRI-STATE Outputs
B ₀ -B ₇	Side B Inputs or TRI-STATE Outputs

Connection Diagram

Pin Assignment for
SOIC and QSOP



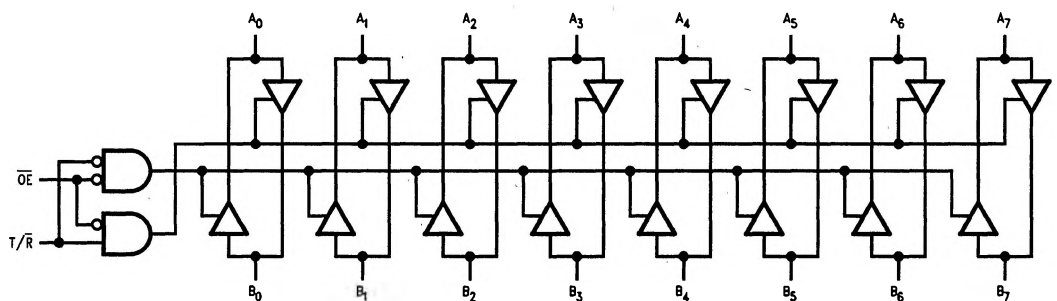
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	SOIC JEDEC	QSOP
Order Number	74LVXC3245WM 74LVXC3245WMX	74LVXC3245QSC 74LVXC3245QSCX
See NS Package Number	M24B	MQA24

Truth Table

Inputs		Outputs
$\overline{OE}$	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

Logic Diagram



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CCA} , V_{CCB})	-0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, $T/\overline{R}$	-0.5V to V_{CCA} + 0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A_n	-0.5V to V_{CCA} + 0.5V
@ B_n	-0.5V to V_{CCB} + 0.5V
DC Input Diode Curr. (I_{IK}) @ $\overline{OE}$, $T/\overline{R}$	± 20 mA
DC Output Diode Current (I_{OK})	± 50 mA
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	± 50 mA
and Max Current	± 200 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
DC Latch-Up Source or Sink Current	± 300 mA

Recommended Operating Conditions

Supply Voltage V_{CCA}	2.7V to 3.6V ($V_{CCA} \leq V_{CCB}$)
V_{CCB}	3.0V to 5.5V
Input Voltage (V_I) @ $\overline{OE}$, $T/\overline{R}$	0V to V_{CCA}
Input Output Voltage ($V_{I/O}$)	
@ A_n	0V to V_{CCA}
@ B_n	0V to V_{CCB}
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Electrical Characteristics

Symbol	Parameter		V _{CCA} (V)	V _{CCB} (V)	74LVXC3245		74LVXC3245		Units	Conditions
					T _A = 25°C		T _A = −40°C to +85°C			
					Typ	Guaranteed Limits				
V _{IHA}	Minimum High Level Input Voltage	A _n	2.7	3.0		2.0	2.0	V	V _{OUT} ≤ 0.1V or ≥ V _{CC} − 0.1V	
		OE	3.0	3.6		2.0	2.0			
		T/ $\overline{R}$	3.6	5.5		2.0	2.0			
V _{IHB}		B _n	2.7	3.0		2.0	2.0			
			3.0	3.6		2.0	2.0			
			3.6	5.5		3.85	3.85			
V _{ILA}	Maximum Low Level Input Voltage	A _n	2.7	3.0		0.8	0.8	V	V _{OUT} ≤ 0.1V or ≥ V _{CC} − 0.1V	
		OE	3.0	3.6		0.8	0.8			
		T/ $\overline{R}$	3.6	5.5		0.8	0.8			
V _{ILB}		B _n	2.7	3.0		0.8	0.8			
			3.0	3.6		0.8	0.8			
			3.6	5.5		1.65	1.65			
V _{OHA}	Minimum High Level Output Voltage		3.0	3.0	2.99	2.9	2.9	V	I _{OUT} = −100 μA I _{OH} = −12 mA I _{OH} = −24 mA I _{OH} = −12 mA I _{OH} = −24 mA	
			3.0	3.0	2.85	2.56	2.46			
			3.0	3.0	2.65	2.35	2.25			
			2.7	3.0	2.5	2.3	2.2			
			2.7	4.5	2.3	2.1	2.0			
V _{OHB}			3.0	3.0	2.99	2.9	2.9	V	I _{OUT} = −100 μA I _{OH} = −12 mA I _{OH} = −24 mA I _{OH} = −12 mA I _{OH} = −24 mA	
			3.0	3.0	2.85	2.56	2.46			
			3.0	3.0	2.65	2.35	2.25			
			3.0	4.5	4.25	3.86	3.76			
V _{OLA}	Maximum Low Level Output Voltage		3.0	3.0	0.002	0.1	0.1	V	I _{OUT} = 100 μA I _{OL} = 24 mA I _{OL} = 12 mA I _{OL} = 24 mA	
			3.0	3.0	0.21	0.36	0.44			
			2.7	3.0	0.11	0.36	0.44			
			2.7	4.5	0.22	0.42	0.5			
V _{OLB}			3.0	3.0	0.002	0.1	0.1	V	I _{OUT} = 100 μA I _{OL} = 24 mA I _{OL} = 24 mA	
			3.0	3.0	0.21	0.36	0.44			
			3.0	4.5	0.18	0.36	0.44			

DC Electrical Characteristics (Continued)

Symbol	Parameter		V _{CCA} (V)	V _{CCB} (V)	74LVXC3245		74LVXC3245		Units	Conditions
					T _A = +25°C		T _A = −40°C to +85°C			
					Typ	Guaranteed Limits				
I _{IN}	Maximum Input Leakage Current @ OE, T/R		3.6 3.6	3.6 5.5		±0.1 ±0.1	±1.0 ±1.0	μA	V _I = V _{CCA} , GND	
I _{OZA}	Maximum TRI-STATE Output Leakage @ A _n		3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	V _I = V _{IL} , V _{IH} , OE = V _{CCA} , V _O = V _{CCA} , GND	
I _{OZB}	Maximum TRI-STATE Output Leakage @ B _n		3.6 3.6	3.6 5.5		±0.5 ±0.5	±5.0 ±5.0	μA	V _I = V _{IL} , V _{IH} , OE = V _{CCA} , V _O = V _{CCB} , GND	
ΔI _{CC}	Maximum I _{CC} /Input	B _n	3.6	5.5	1.0	1.35	1.5	mA	V _I = V _{CCB} −2.1V	
		All Inputs	3.6	3.6		0.35	0.5		V _I = V _{CC} −0.6V	
I _{CCA1}	Quiescent V _{CCA} Supply Current as B Port Floats		3.6	Open		5	50	μA	A _n = V _{CCA} or GND B _n = Open, OE = V _{CCA} , T/R = V _{CCA} , V _{CCB} = Open	
I _{CCA2}	Quiescent V _{CCA} Supply Current		3.6 3.6	3.6 5.5		5 5	50 50	μA	A _n = V _{CCA} or GND, B _n = V _{CCB} or GND, OE = GND, T/R = GND	
I _{CCB}	Quiescent V _{CCB} Supply Current		3.6 3.6	3.6 5.5		5 8	50 80	μA	A _n = V _{CCA} or GND, B _n = V _{CCB} or GND, OE = GND, T/R = V _{CCA}	
VOLPA	Quiet Output Maximum Dynamic		3.3 3.3	3.3 5.0		0.8 0.8		V	(Notes 1, 2)	
VOLPB	VOL		3.3 3.3	3.3 5.0		0.8 1.5		V	(Notes 1, 2)	
VOLVA	Quiet Output Minimum Dynamic		3.3 3.3	3.3 5.0		−0.8 −0.8		V	(Notes 1, 2)	
VOLVB	VOL		3.3 3.3	3.3 5.0		−0.8 −1.2		V	(Notes 1, 2)	
V _{IHDA}	Minimum High Level Dynamic		3.3 3.3	3.3 5.0		2.0 2.0		V	(Notes 1, 3)	
V _{IHDB}	Input Voltage		3.3 3.3	3.3 5.0		2.0 3.5		V	(Notes 1, 3)	
V _{ILDA}	Maximum Low Level Dynamic		3.3 3.3	3.3 5.0		0.8 0.8		V	(Notes 1, 3)	
V _{ILDB}	Input Voltage		3.3 3.3	3.3 5.0		0.8 1.5		V	(Notes 1, 3)	

Note 1: Worst case package.

Note 2: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 3: Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), 0V to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	74LVXC3245			74LVXC3245		74LVXC3245			74LVXC3245		Units
		$T_A = +25^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}-3.6\text{V}$ $V_{CCB} = 4.5\text{V}-5.5\text{V}$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}-3.6\text{V}$ $V_{CCB} = 4.5\text{V}-5.5\text{V}$		$T_A = +25^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}-3.6\text{V}$ $V_{CCB} = 3.0\text{V}-3.6\text{V}$			$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50\text{ pF}$ $V_{CCA} = 2.7\text{V}-3.6\text{V}$ $V_{CCB} = 3.0\text{V}-3.6\text{V}$		
		Min	Typ (Note 1)	Max	Min	Max	Min	Typ (Note 2)	Max	Min	Max	
t _{PHL}	Propagation Delay	1.0	4.8	8.0	1.0	8.5	1.0	5.5	8.5	1.0	9.0	ns
t _{PLH}	A to B	1.0	3.9	6.5	1.0	7.0	1.0	5.2	8.0	1.0	8.5	
t _{PHL}	Propagation Delay	1.0	3.8	6.5	1.0	7.0	1.0	4.4	7.0	1.0	7.5	ns
t _{PLH}	B to A	1.0	4.3	7.5	1.0	8.0	1.0	5.1	7.5	1.0	8.0	
t _{PZL}	Output Enable Time	1.0	4.7	8.0	1.0	8.5	1.0	6.0	9.0	1.0	9.5	ns
t _{PZH}	OE to B	1.0	4.8	8.5	1.0	9.0	1.0	6.1	9.5	1.0	10.0	
t _{PZL}	Output Enable Time	1.0	5.9	9.5	1.0	10.0	1.0	6.4	10.0	1.0	10.5	ns
t _{PZH}	OE to A	1.0	5.4	9.0	1.0	9.5	1.0	5.8	9.0	1.0	9.5	
t _{PHZ}	Output Disable Time	1.0	4.0	8.0	1.0	8.5	1.0	6.3	9.5	1.0	10.0	ns
t _{PLZ}	OE to B	1.0	3.8	7.5	1.0	8.0	1.0	4.5	8.0	1.0	8.5	
t _{PHZ}	Output Disable Time	1.0	4.6	9.5	1.0	10.0	1.0	5.2	9.5	1.0	10.0	ns
t _{PLZ}	OE to A	1.0	3.1	6.5	1.0	7.0	1.0	3.4	6.5	1.0	7.0	
t _{OSHL}	Output to Output	1.0 1.5			1.5		1.0 1.5			1.5		ns
t _{OSLH}	Skew* Data to Output											

Note 1: Typical values at $V_{CCA} = 3.3\text{V}$, $V_{CCB} = 5.0\text{V}$ @ 25°C .

Note 2: Typical values at $V_{CCA} = 3.3\text{V}$, $V_{CCB} = 3.3\text{V}$ @ 25°C .

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

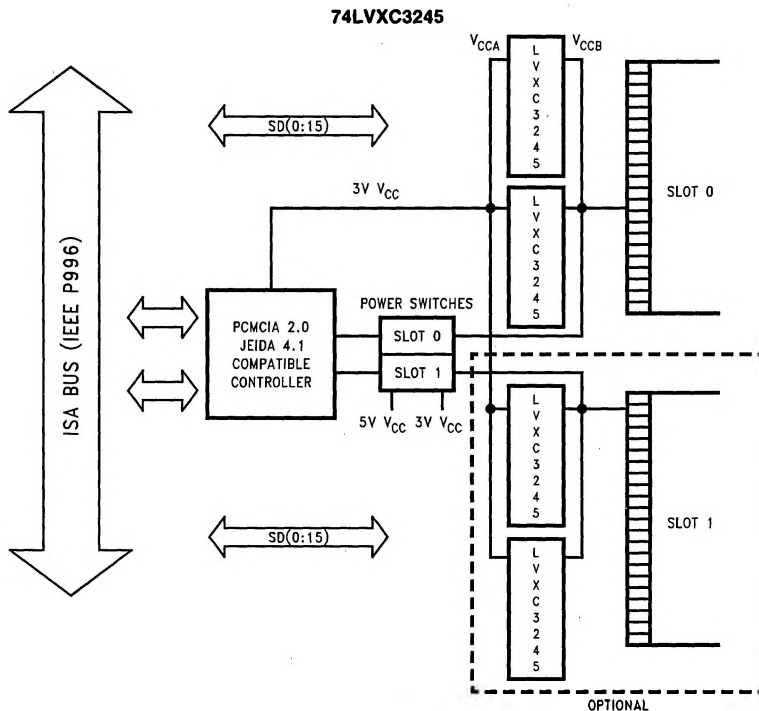
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{CCA} = 3.3\text{V}$ $V_{CCB} = 5.0\text{V}$
C_{PD}	Power Dissipation Capacitance	$A \rightarrow B$	50	pF
		$B \rightarrow A$	40	pF

C_{PD} is measured at 10 MHz.

Configurable I/O Application for PCMCIA Cards

Block Diagram



TL/F/12008-3

The LVXC3245 is a 24-pin dual supply device well suited for PCMCIA configurable I/O applications. Ideal for low power notebook designs, the LVXC3245 consumes less than 1 mW of quiescent power in all modes of operation. The LVXC3245 meets all PCMCIA I/O voltage requirements at 5V and 3.3V operation. By tying V_{CCB} of the LVXC3245 to the card voltage supply, the PCMCIA card will always experience rail to rail output swings, maximizing the reliability of the interface.

The V_{CCA} pin on the LVXC3245 must always be tied to a 3V power supply. This voltage connection provides internal references needed to account for variations in V_{CCB}. When connected as in the figure above, the LVXC3245 meets all the voltage and current requirements of the ISA bus standard (IEEE P996).