



74LVQ240

Low Voltage Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

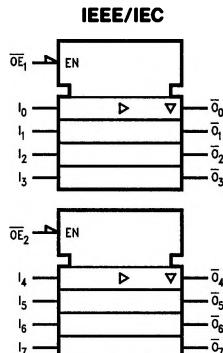
The LVQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- Ideal for low power/low noise 3.3V applications
- Implements patented Quiet Series EMI reduction circuitry
- Available in SOIC JEDEC, SOIC EIAJ and QSOP packages
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4 kV minimum ESD immunity
- MIL-STD-883 54ACQ products are available for Military/Aerospace applications

Ordering Code: See Section 11

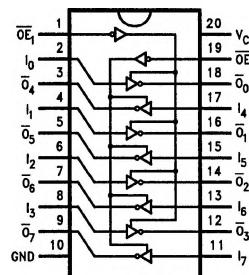
Logic Symbol



TL/F/11611-1

Connection Diagram

Pin Assignment,
SOIC and QSOP



TL/F/11611-2

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)	
\overline{OE}_1	I_n		
L	L	H	
L	H	L	
H	X	Z	

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$ I_0-I_7 $\overline{O}_0-\overline{O}_7$	TRI-STATE Output Enable Inputs Inputs Outputs

Inputs		Outputs (Pins 3, 5, 7, 9)	
\overline{OE}_2	I_n		
L	L	H	
L	H	L	
H	X	Z	

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

	SOIC JEDEC	SOIC EIAJ	SSOP JEDEC
Order Number	74LVQ240SC 74LVQ240SCX	74LVQ240SJ 74LVQ240SJX	74LVQ240QSC 74LVQ240SCX
See NS Package Number	M20B	M20D	MQA20

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	$-0.5V$ to $+7.0V$
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	$+20\text{ mA}$
DC Input Voltage (V_I)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	$+20\text{ mA}$
DC Output Voltage (V_O)	$-0.5V$ to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	$\pm 50\text{ mA}$
DC V_{CC} or Ground Current (I_{CC} or I_{GND})	$\pm 400\text{ mA}$
Storage Temperature (T_{STG})	-65°C to $+150^{\circ}\text{C}$
DC Latch-Up Source or Sink Current	$\pm 300\text{ mA}$

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

DC Characteristics

Symbol	Parameter	V_{CC} (V)	74LVQ240		74LVO240	Units	Conditions
			$T_A = +25^{\circ}\text{C}$		$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	2.0	V	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	0.8	V	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50\text{ }\mu\text{A}$
		3.0		2.58	2.48	V	* $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12\text{ mA}$
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50\text{ }\mu\text{A}$
		3.0		0.36	0.44	V	* $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12\text{ mA}$
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	± 1.0	μA	$V_I = V_{CC}, \text{GND}$

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	74LVQ240		Units	Conditions		
			T _A = +25°C					
			Typ	Guaranteed Limits				
I _{OLD}	†Minimum Dynamic Output Current	3.6		36	mA	V _{OLD} = 0.8V Max (Note 1)		
I _{OHD}		3.6		-25	mA	V _{OHD} = 2.0V Min (Note 1)		
I _{CC}	Maximum Quiescent Supply Current	3.6		4.0	μA	V _{IN} = V _{CC} or GND		
I _{OZ}	Maximum TRI-STATE Leakage Current	3.6		±0.25	μA	V _{I(OE)} = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.4	0.8	V	(Notes 2, 3)		
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	-0.4	-0.8	V	(Notes 2, 3)		
V _{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.6	2.0	V	(Notes 2, 4)		
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.6	0.8	V	(Notes 2, 4)		

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed for 74LVQ.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n - 1 Inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	74LVQ240			Units		
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max			
t _{PHL} , t _{PLH}	Propagation Delay Data to Output	2.7 3.3 ± 0.3	2.0 2.0	8.4 7.0	14.0 10.0	2.0 2.0	15.0 10.5	ns
t _{PZL} , t _{PZH}	Output Enable Time	2.7 3.3 ± 0.3	2.5 2.5	9.6 8.0	16.9 12.0	2.5 2.5	18.0 12.5	ns
t _{PHZ} , t _{PLZ}	Output Disable Time	2.7 3.3 ± 0.3	1.0 1.0	10.2 8.5	19.0 13.5	1.0 1.0	20.0 14.0	ns
t _{OShL} , t _{OSLH}	Output to Output Skew *Data to Output	2.7 3.3 ± 0.3		1.0 1.0	1.5 1.5		1.5 1.5	ns

*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OShL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = \text{Open}$
C_{PD} (Note 1)	Power Dissipation Capacitance	70	pF	$V_{CC} = 3.3V$

Note 1: C_{PD} is measured at 10 MHz.