



74LCX374

Low-Voltage Octal D Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX374 consists of eight D-type flip-flops featuring separate D-type inputs for each flip-flop and TRI-STATE® outputs for bus-oriented applications. A buffered clock (CP) and Output Enable (OE) are common to all flip-flops. The LCX374 is designed for low-voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

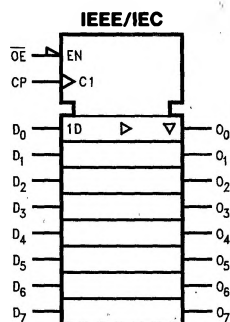
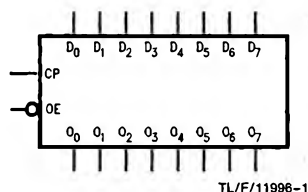
The LCX374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

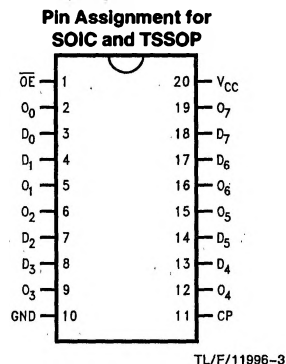
- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC, SOIC EIAJ and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 374
- Latchup performance exceeds 300 mA
- ESD performance:
 - Human Body Model > 2000V
 - Machine Model > 250V

Ordering Code: See Section 11

Logic Symbols



Connection Diagram



Pin Names	Description
D ₀ –D ₇	Data Inputs
CP	Clock Pulse Input
OE	Output Enable Input
Q ₀ –Q ₇	TRI-STATE Outputs

	SOIC JEDEC	SOIC EIAJ	TSSOP JEDEC
Order Number	74LCX374WM 74LCX374WMX	74LCX374SJ 74LCX374SJX	74LCX374MTCX
See NS Package Number	M20B	M20D	MTC20

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Functional Description

The LCX374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H		L	H
L		L	L
X	L	L	O_0
X	X	H	Z

H = HIGH Voltage Level

L = LOW Voltage Level

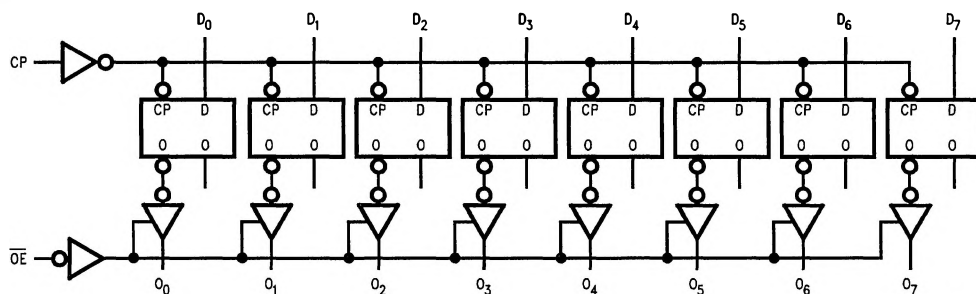
X = Immaterial

Z = High Impedance

 = LOW-to-HIGH Transition

O_0 = Previous O_0 before HIGH to LOW of CP

Logic Diagram



TL/F/11996-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_I)	-0.5V to +7.0V
Output Voltage (V_O)	
Outputs TRI-STATE	-0.5V to +7.0V
Outputs Active (Note 2)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK}) $V_I < 0$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	
Output in Active State	0V to V_{CC}
Output in "OFF" State	0V to 5.5V
Output Current I_{OH}/I_{OL}	
$V_{CC} = 3.0V$ to $3.6V$	±24 mA
$V_{CC} = 2.7V$ to $3.0V$	±12 mA
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Ratge ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to $2.0V$, $V_{CC} = 3.0V$	10 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Max		
V_{IH}	High Level Input Voltage	2.7-3.6	2.0		V	$V_{OUT} \leq 0.1V$ or $\geq V_{CC} - 0.1V$
V_{IL}	Low Level Input Voltage	2.7-3.6		0.8		
V_{OH}	High Level Output Voltage	2.7-3.6 2.7 3.0 3.0	$V_{CC} - 0.2$ 2.2 2.4 2.2		V	$I_{OH} = -100 \mu A$ $I_{OH} = -12 \text{ mA}$ $I_{OH} = -18 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
V_{OL}	Low Level Output Voltage	2.7-3.6 2.7 3.0		0.2 0.4 0.55	V	$I_{OL} = 100 \mu A$ $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
I_I	Input Leakage Current	2.7-3.6		±5.0	μA	$0 \leq V_I \leq 5.5V$
I_{OZ}	TRI-STATE Output Leakage	2.7-3.6		±5.0	μA	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or V_{IL}
I_{OFF}	Power Off Leakage Current	0		100	μA	V_I or $V_O = 5.5V$
I_{CC}	Quiescent Supply Current	2.7-3.6		10	μA	$V_I = V_{CC}$ or GND
				±10	μA	$3.6 \leq (V_I, V_O) \leq 5.5V$
ΔI_{CC}	Increase in I_{CC} per Input	2.7-3.6		500	μA	$V_{IH} = V_{CC} - 0.6V$

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Max (Note 2)	
t _{PHL} t _{PLH}	Propagation Delay CP to Output	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t _{PZH} t _{PZL}	Output Enable Time	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time	2.7 3.0–3.6	1.5 1.5	8.5 7.5	ns
t _S	Setup Time	2.7 3.0–3.6	2.5 2.5		ns
t _H	Hold Time	2.7 3.0–3.6	1.5 1.5		ns
t _W	Pulse Width	2.7 3.0–3.6	4.0 4.0		ns
t _{OSHL} , t _{OSLH}	Output to Output Skew (Note 1)	3.0		1.0	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	T _A = 25°C	Units	Conditions
			Typical		
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	0.8	V	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	3.3	0.8	V	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V

Capacitance

Symbol	Parameter	Typical	Units	Conditions
C _{IN}	Input Capacitance	7	pF	V _{CC} = Open V _I = 0V or V _{CC}
C _{OUT}	Output Capacitance	8	pF	V _{CC} = 3.3V V _I = 0V or V _{CC}
C _{PD}	Power Dissipation Capacitance	32	pF	V _{CC} = 3.3V V _I = 0V or V _{CC} F = 10 MHz