



CY54/74FCT540T CY54/74FCT541T

8-Bit Buffers/Line Drivers

Features

- Function, pinout and drive compatible with FCT and F logic
- FCT-C speed at 4.1 ns max. (Com'l)
- FCT-A speed at 4.8 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V

- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l), 48 mA (Mil)
- Source current 32 mA (Com'l), 12 mA (Mil)
- Three-state outputs

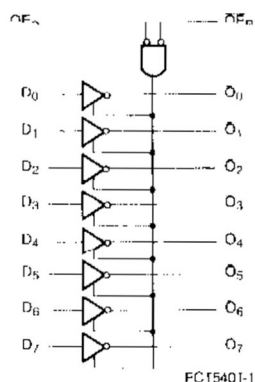
Functional Description

The FCT540T inverting buffer/line driver and the FCT541T non-inverting buffer/line driver are designed to be

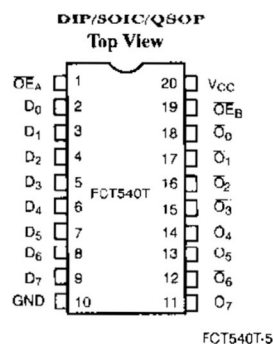
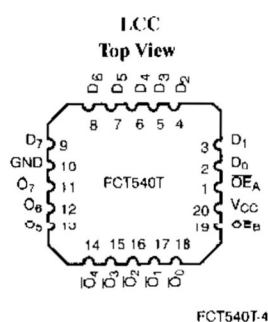
employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers. The devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

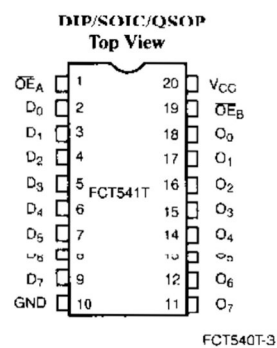
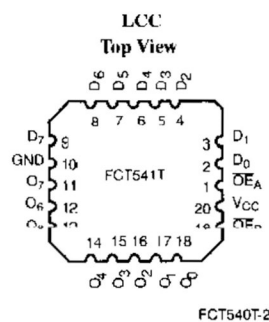
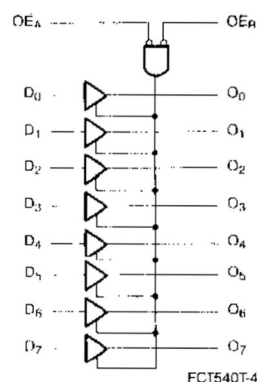
Logic Block Diagram – FCT540T



Pin Configurations



Logic Block Diagram – FCT541T





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Capacitance^[9]

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance		5	10	pF
C _{OUT}	Output Capacitance		9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
AI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} =Max., V _{IN} =3.4V ^[8] f _I =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f _I =10 MHz, OE _A =OE _B =GND, or OE _A =GND, OE _B =V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/ MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f _I =10 MHz, OE _A =OE _B =GND, or OE _A =GND, OE _B =V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, One Bit Toggling at f _I =10 MHz, OE _A =OE _B =GND, or OE _A =GND, OE _B =V _{CC} , V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f _I =2.5 MHz, OE _A =OE _B =GND, or OE _A =GND, OE _B =V _{CC} , V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	1.3	2.6 ^[11]	mA
		V _{CC} =Max., 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f _I =2.5 MHz, OE _A =OE _B =GND, or OE _A =GND, OE _B =V _{CC} , V _{IN} =3.4V or V _{IN} =GND	3.3	10.6 ^[11]	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.

9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + AI_{CC} \cdot D_{IH} N_I + I_{CCD} (f_I/2 + f_I N_I)$
I_{CC} = Quiescent Current with CMOS input levels
AI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_{IH} = Duty Cycle for TTL inputs HIGH

N_T = Number of TTL inputs at D_{IH}

I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

f_I = Clock frequency for registered devices, otherwise zero

f_I = Input signal frequency

N_I = Number of inputs changing at f_I

All currents are in milliamps and all frequencies are in megahertz.

11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.



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Switching Characteristics Over the Operating Range

Switching Characteristics Over the Operating Range											
Parameter	Description	FCT540T/FCT541T				FCT540AT/FCT541AT				Unit	Fig. No. ^[1,3]
		Military		Commercial		Military		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output (FCT540)	1.5	9.5	1.5	8.5	1.5	5.1	1.5	4.8	ns	1, 2
t _{PLH} t _{PHL}	Propagation Delay Data to Output (FCT541)	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	ns	1, 7, 8

Parameter	Description	FCT540CT/FCT541CT				FCT540DT/ FCT541DT		Unit	Fig. No. ^[1,3]
		Military		Commercial		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay Data to Output (FCT540)	1.5	4.7	1.5	4.1	1.5	3.8	ns	1, 2
t _{PLH} t _{PHL}	Propagation Delay Data to Output (FCT541)	1.5	4.6	1.5	4.1	1.5	3.3	ns	1, 3
t _{PZH} t _{PZL}	Output Enable Time	1.5	6.5	1.5	5.8	1.5	5.2	ns	1, 7, 8
t _{PHZ} t _{PLZ}	Output Disable Time	1.5	5.7	1.5	5.2	1.5	5.0	ns	1, 7, 8

Shaded areas contain preliminary information.

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays. 13. See "Parameter Measurement Information" in the General Information section.



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CY54/74FCT541T

Ordering Information—FCT540T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT540DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT540DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT540CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.7	CY54FCT540CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT540ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT540ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.5	CY74FCT540TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT540TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT540TSOC	S5	20-Lead (300-Mil) Molded SOIC	
9.5	CY54FCT540TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT540TLMB	L61	20-Pin Square Leadless Chip Carrier	

Ordering Information—FCT541T

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.8	CY74FCT541DTQC	Q5	20-Lead (150-Mil) QSOP	Commercial
	CY74FCT541DTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.1	CY74FCT541CTPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541CTQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541CTSOC	S5	20-Lead (300-Mil) Molded SOIC	
4.6	CY54FCT541CTDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541CTLMB	L61	20-Pin Square Leadless Chip Carrier	
4.8	CY74FCT541ATPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541ATQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541ATSOC	S5	20-Lead (300-Mil) Molded SOIC	
5.1	CY54FCT541ATDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541ATLMB	L61	20-Pin Square Leadless Chip Carrier	
8.0	CY74FCT541TPC	P5	20-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT541TQC	Q5	20-Lead (150-Mil) QSOP	
	CY74FCT541TSOC	S5	20-Lead (300-Mil) Molded SOIC	
9.0	CY54FCT541TDMB	D6	20-Lead (300-Mil) CerDIP	Military
	CY54FCT541TLMB	L61	20-Pin Square Leadless Chip Carrier	

Shaded areas contain preliminary information.

Document #: 38-00260-A