National Semiconductor

54AC/74AC251 • 54ACT/74ACT251
8-Input Multiplexer with TRI-STATE® Output

General Description

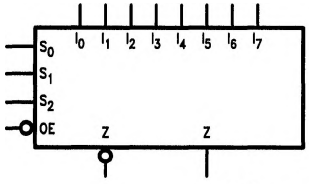
The 'AC/'ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Multifunctional capability
- On-chip select logic decoding
- Inverting and noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT251 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC251: 5962-87692
  - — 'ACT251: 5962-89599

Ordering Code: See Section 8

Logic Symbols



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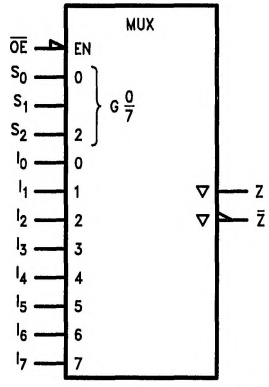
IEEE/IEC



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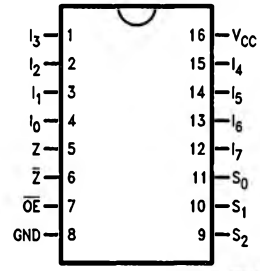
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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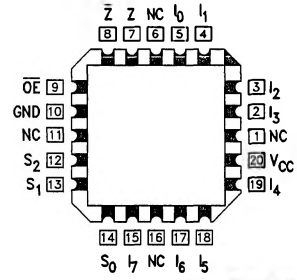
Pin Assignment for LCC



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Pin Names	Description
S_0–S_2	Select Inputs
$\overline{OE}$	TRI-STATE Output Enable Input
I_0–I_7	Multiplexer Inputs
Z	TRI-STATE Multiplexer Output
$\overline{Z}$	Complementary TRI-STATE Multiplexer Output

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

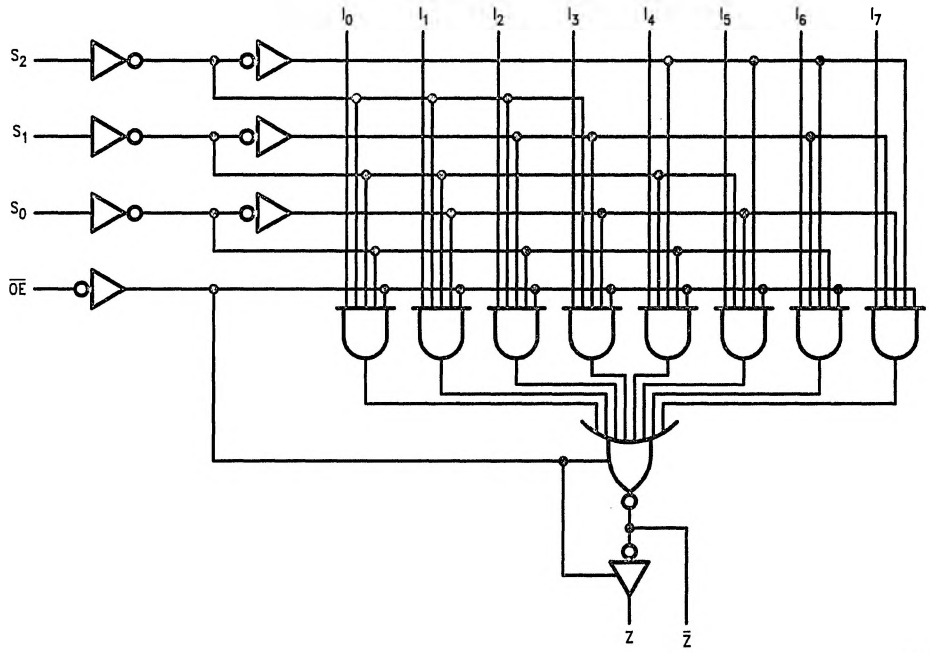
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

Truth Table

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C Typ	74AC T_A = +25°C Guaranteed Limits	54AC T_A = −55°C to +125°C Guaranteed Limits	74AC T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C Typ	74AC T_A = +25°C Guaranteed Limits	54AC T_A = −55°C to +125°C Guaranteed Limits	74AC T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C Typ	74ACT T_A = +25°C Guaranteed Limits	54ACT T_A = −55°C to +125°C Guaranteed Limits	74ACT T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.5	11.5	17.5	1.0	21.0	1.5	19.0	ns	2-3,4
		5.0	1.5	8.5	12.5	1.0	15.5	1.5	13.5		
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.5	11.0	17.5	1.0	21.0	1.5	19.0	ns	2-3,4
		5.0	1.5	8.0	12.5	1.0	15.5	1.5	13.5		
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.5	10.0	14.0	1.0	17.0	1.5	15.5	ns	2-3,4
		5.0	1.5	7.0	10.0	1.0	12.0	1.5	11.0		
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.5	9.0	14.0	1.0	16.5	1.5	15.5	ns	2-3,4
		5.0	1.5	6.5	10.0	1.0	12.0	1.5	11.0		
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.5	11.0	1.0	13.0	1.5	12.0	ns	2-5
		5.0	1.5	5.5	8.0	1.0	10.0	1.5	9.0		
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.5	11.0	1.0	13.0	1.5	12.0	ns	2-6
		5.0	1.5	5.5	8.0	1.0	10.0	1.5	9.0		
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	8.5	11.5	3.5	14.0	1.5	13.0	ns	2-5
		5.0	1.5	7.0	9.5	2.5	11.0	1.5	10.0		
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.0	11.0	4.0	13.0	1.5	12.0	ns	2-6
		5.0	1.5	5.5	8.0	3.0	10.0	1.5	8.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	2.5	7.0	15.5	1.0	18.5	2.0	17.0	ns	2-3,4
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	2.5	7.5	16.5	1.0	19.5	2.5	18.5	ns	2-3,4
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	2.5	5.5	12.0	1.0	14.0	2.0	13.0	ns	2-3,4
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	2.5	6.5	12.5	1.0	15.0	2.5	14.0	ns	2-3,4
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.5	5.0	8.5	1.0	10.0	1.5	9.0	ns	2-5
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.5	4.5	8.5	1.0	10.0	1.5	9.5	ns	2-6
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	2.0	6.0	12.0	1.0	13.5	2.0	13.0	ns	2-5
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.5	4.5	8.5	1.0	9.5	1.5	9.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	70.0	pF	V_{CC} = 5.0V